0400

4-17-01

Attorney's Docket No.: 774-010234-US(PAR)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: OOI et al.
Serial No.: 09/802,084
Filed: 3/08/01
For: QUANTUM WELL INTERMIXING

Group No.:

Examiner:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

TRANSMITTAL OF CERTIFIED COPY

Attached please find the certified copy of the foreign application from which priority is claimed for this case:

Country	**: Singapore**
Application Number	**: PCT/SG00/00039**
Filing Date	**: 8 March 2000**

WARNING: "When a document that is required by statute to be certified must be filed, a copy, including a photocopy or facsimile transmission of the certification is not acceptable." 37 CFR 1.4(b) (emphasis added.)

SIGNATURE OF ATTORNEY

Reg. No.: 24,622

Clarence A. Green

Type or print name of attorney

Tel. No.: (203) 259-1800

Perman & Green, LLP

Customer No.: 2512

P.O. Address

425 Post Road, Fairfield, CT 06430

NOTE: The claim to priority need be in no special form and may be made by the attorney or agent if the foreign application is referred to in the oath or declaration as required by § 1.63.

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8a)

I hereby certify that this correspondence is, on the date shown below, being:

☒ MAILING

deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231

Date: 4/27/01

☐ FACSIMILE

transmitted by facsimile to the Patent and Trademark Office

Deborah J. Clark

Signature

DEBORAH J. CLARK

(type or print name of person certifying)

REGISTRY OF PATENTS
SINGAPORE

This is to certify that the annexed is a true copy of the following Singapore patent application as filed in this Registry.

Date of Filing	:	08 MAR 2000
Application number	:	PCT/SG00/00039
Applicants	:	NANYANG TECHNOLOGICAL UNIVERSITY
Title of Invention	:	PLASMA BASED PROCESS FOR PHOTONIC INTEGRATION

I further certify that the annexed documents are not, as yet, open to public inspection.

Tan Kar Leng (Ms)
Assistant Registrar
for REGISTRAR OF PATENT
SINGAPORE

15 March 2001

PCT REQUEST

TC5000605WOF

Original (for **SUBMISSION**) - printed on 07.03.2000 02:41:16 AM

0	**For receiving Office use only**	
0-1	International Application No.	PCT//SG 0 0 / 0 0 0 3 9
0-2	International Filing Date	0 8 MAR 2000 (08-03-00)
0-3	Name of receiving Office and "PCT International Application"	REGISTRY OF PATENTS (SINGAPORE) PCT INTERNATIONAL APPLICATION
0-4	**Form - PCT/RO/101 PCT Request**	
0-4-1	Prepared using	PCT-EASY Version 2.90 (updated 01.01.2000)
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	Intellectual Property Office of Singapore (RO/SG)
0-7	**Applicant's or agent's file reference**	TC5000605WOF
I	**Title of invention**	PLASMA BASED PROCESS FOR PHOTONIC INTEGRATION
II	**Applicant**	
II-1	This person is:	applicant only
II-2	Applicant for	all designated States except US
II-4	Name	NANYANG TECHNOLOGICAL UNIVERSITY
II-5	Address:	SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING NANYANG AVENUE 639 798 SINGAPORE Singapore
II-6	State of nationality	SG
II-7	State of residence	SG
II-8	Telephone No.	-
II-9	Facsimile No.	-
II-10	e-mail	-
III-1	**Applicant and/or inventor**	
III-1-1	This person is:	applicant and inventor
III-1-2	Applicant for	US only
III-1-4	Name (LAST, First)	OOI, Boon, Siew
III-1-5	Address:	35F, NANYANG AVENUE #10-11 639 808 SINGAPORE Singapore
III-1-6	State of nationality	MY
III-1-7	State of residence	SG

PCT REQUEST TC5000605WOF

Original (for **SUBMISSION**) - printed on 07.03.2000 02:41:16 AM

III-2	**Applicant and/or inventor**	
III-2-1	This person is:	applicant and inventor
III-2-2	Applicant for	US only
III-2-4	Name (LAST, First)	LAM, Yee, Loy
III-2-5	Address:	Block 271 #14-261 Choa Chu Kang Avenue 2 680 271 SINGAPORE Singapore
III-2-6	State of nationality	SG
III-2-7	State of residence	SG
III-3	**Applicant and/or inventor**	
III-3-1	This person is:	applicant and inventor
III-3-2	Applicant for	US only
III-3-4	Name (LAST, First)	ZHOU, Yan
III-3-5	Address:	3 BUKIT BATOK STREET 25 #06-04 658 881 SINGAPORE Singapore
III-3-6	State of nationality	SG
III-3-7	State of residence	SG
III-4	**Applicant and/or inventor**	
III-4-1	This person is:	applicant and inventor
III-4-2	Applicant for	US only
III-4-4	Name (LAST, First)	CHAN, Yuen, Chuen
III-4-5	Address:	BLOCK 52, LENGKOK BAHRU #02-309 150 052 SINGAPORE Singapore
III-4-6	State of nationality	SG
III-4-7	State of residence	SG
III-5	**Applicant and/or inventor**	
III-5-1	This person is:	applicant and inventor
III-5-2	Applicant for	US only
III-5-4	Name (LAST, First)	NG, Geok, Ing
III-5-5	Address:	BLOCK 371, CLEMENTI AVENUE 4, #07-288 120 371 SINGAPORE Singapore
III-5-6	State of nationality	SG
III-5-7	State of residence	SG

PCT REQUEST TC5000605WOF

Original (for **SUBMISSION**) - printed on 07.03.2000 02:41:16 AM

IV-1	**Agent or common representative; or address for correspondence** The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	agent
IV-1-1	Name (LAST, First)	NAMAZIE, Farah
IV-1-2	Address:	HAQ & NAMAZIE PARTNERSHIP ROBINSON ROAD, P.O. BOX 765 901 515 SINGAPORE Singapore
IV-1-3	Telephone No.	(65) 4386613
IV-1-4	Facsimile No.	(65) 438 7383, (65) 438 7393
IV-1-5	e-mail	hnlegal@cyberway.com.sg
IV-2	**Additional agent(s)**	additional agent(s) with same address as first named agent
IV-2-1	Name(s)	HAQ, Murgiana; HAQ, Tasneem; LOKE, Adrian
V	**Designation of States**	
V-1	Regional Patent (other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned)	EP: AT BE CH&LI CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE and any other State which is a Contracting State of the European Patent Convention and of the PCT
V-2	National Patent (other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned)	CA JP KR SG US
V-5	**Precautionary Designation Statement** In addition to the designations made under items V-1, V-2 and V-3, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except any designation(s) of the State(s) indicated under item V-6 below. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit.	
V-6	**Exclusion(s) from precautionary designations**	NONE
VI	**Priority claim**	NONE
VII-1	**International Searching Authority Chosen**	European Patent Office (EPO) (ISA/EP)

PCT REQUEST

TC5000605WOF

Original (for **SUBMISSION**) - printed on 07.03.2000 02:41:16 AM

VIII	Check list	number of sheets	electronic file(s) attached
VIII-1	Request	4	-
VIII-2	Description	20	-
VIII-3	Claims	4	-
VIII-4	Abstract	1	abstract.txt
VIII-5	Drawings	13	-
VIII-7	TOTAL	42	
	Accompanying items	paper document(s) attached	electronic file(s) attached
VIII-8	Fee calculation sheet	✓	-
VIII-9	Separate signed power of attorney	✓	-
VIII-16	PCT-EASY diskette	-	diskette
VIII-18	**Figure of the drawings which should accompany the abstract**	FIGURE 8 AND FIGURE 9	
VIII-19	**Language of filing of the international application**	English	
IX-1	**Signature of applicant or agent**		
IX-1-1	Name (LAST, First)	NAMAZIE, Farah	

FOR RECEIVING OFFICE USE ONLY

10-1	**Date of actual receipt of the purported international application**	08 MAR 2000 (08-03-00)
10-2	**Drawings:**	
10-2-1	Received	
10-2-2	Not received	
10-3	**Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application**	
10-4	**Date of timely receipt of the required corrections under PCT Article 11(2)**	
10-5	**International Searching Authority**	ISA/EP
10-6	**Transmittal of search copy delayed until search fee is paid**	

FOR INTERNATIONAL BUREAU USE ONLY

11-1	**Date of receipt of the record copy by the International Bureau**	

PLASMA BASED PROCESS FOR PHOTONIC INTEGRATION

Field of the Invention

The present invention relates to a method of manufacturing a photonic integrated circuit by quantum well intermixing and to a photonic integrated circuit produced by the method.

Background of the Invention

It is now established that monolithic integration of photonic and optoelectronic components, such as laser diodes, amplifiers detectors and modulators, is highly desirable. Such integration has the capability of producing higher device yield, improvements in performance and speed, increase in long term reliability and robustness and reduction in chip size, as well as offering significant potential for reduction in costs.

Where an active photonic device such as a semiconductor laser and a passive device such as a waveguide is integrated into a photonic integrated circuit, it is possible to reduce coupling losses, and overall enhance the robustness and functionality of the device.

Such integration can cause difficulties due to the technical processes involved. Furthermore, to reduce absorption of the passive sections it is required to tune the bandgap energy and hence the absorption peak.

Three techniques are established in the art for achieving this. These techniques are:-

1. epitaxial growth and regrowth
2. selective area epitaxy
3. quantum well intermixing

Epitaxial growth and regrowth is a well known technique developed for III V integration. In this technique, shown in Figure 11, a quantum well structure of a desired bandgap is first grown onto a bulk semiconductor substrate (Fig. 11a). Then, the epilayer is etched away at regions in which a structure of a different bandgap is required (Fig. 11b). A new quantum well structure with a different bandgap energy is then grown onto the semiconductor surface (Fig. 11c), thus producing regions of different bandgap energy. In the event where more than two different bandgap energies are required, the growth and regrowth process will be repeated.

However, passive butt coupled waveguides using epitaxial growth and regrowth may suffer from mismatch of mode size and reflection at the interface. Although good mode coupling can be obtained by regrowth of quantum well structures, it is difficult to grow passive waveguides with precise alignment.

Evanescent coupling of waveguide structures grown on bulk using this technique is polarisation sensitive. In addition, evanescent coupling in directional couplers usually has a very tight tolerance which restricts the yield of the process. Quantum well structures grown using the epitaxial growth and regrowth technique can provide gain in the evanescent mode; however it gives poor optical confinement to the waveguides.

These disadvantages prejudice the practicality of the epitaxial growth and regrowth technique.

Selective area epitaxy, also known as epitaxial growth on patterned substrate, involves growth of quantum well structures on the dielectric patterned substrate and varying the quantum well width by adjusting the area in a single growth. As shown in Figure 12, a dielectric mask, typically SiO_2, is firstly coated

onto the substrate, after which slots of different area are patterned on to the dielectric mask (Fig. 12a). The quantum well epilayer is then grown onto the sample (Fig 12 b). Under precise sets of growing condition, no growth takes place on top of the dielectric, but surface migration of the group III species takes place for some distance across the mask to the nearest opening. Thus, according to the different width of the pattern opening on the mask, the thickness of the epilayer grown also varies. The dielectric mask is removed (Fig. 12c) and a quantum well epilayer of different bandgap energy is formed at different parts of the sample. An advantage of this approach is the reduction in total number of processing steps. It enables the essentially optimum laser and modulator multiple quantum well sections to be accomplished in a single epitaxial growth stage. Using this technique, wider quantum wells may be formed on areas with narrow dielectric slots, as the growth rate is higher at these regions. In contrast, where the dielectric slots are wider, the growth rate is low and as a result thin layers of quantum wells with high bandgap energy will grow. By comparison with the above-mentioned epitaxial growth and regrowth technique, the growth step using selective area epitaxy can be reduced. Selective area epitaxy can also be employed to provide a spatial resolution of around 100 m.

Selective area epitaxy however does have disadvantages in that it is complicated and requires undesirably complex steps of sample preparation. In addition, the technique commonly gives non-uniform growth rates across the sample which means that passive waveguide sections are relatively lossy.

The third mentioned technique, quantum well intermixing provides a post-growth and planar bandgap tuning technique for III and V quantum well structures in which the bandgap of the quantum well epilayer is tuned after the epitaxial growth process. Quantum well intermixing is based on the fact that a quantum well is inherently a metastable system due to the large concentration gradient of atomic species across the quantum wells and barriers interface. Hence, this allows the modification of the bandgap of quantum well structures in selected regions by interdiffusing the quantum wells with the barriers to form alloy semiconductors. After quantum well intermixing, the quantum well bandgap structure between the well and the barrier changes from an abrupt profile to a parabolic profile. Thus in most cases, a blue shift occurs of the bandgap energy of the quantum well, i.e., it increases its bandgap energy and reduces its peak absorption wavelength (Figure 13). The bandgap of the intermixed alloy is

generally larger than that of the original quantum well structure, and this provides the ability to form passive photonic and electronic components. It will be seen therefore that the fabrication of monolithic devices using quantum well intermixing can eliminate a series of etching and regrowth processes. The technique can provide good alignment of active and passive waveguides and the possibility of a negligibly small reflection coefficient. The waveguide losses are mainly due to the intrinsic free carrier absorption from the P-I-N structure. The process intrinsically produces mode matching and thus the fabrication of photonic integrated circuits is feasible.

Quantum well intermixing has been successfully used in fabrication of integrated mode-locked semiconductor lasers, low loss waveguides for switches, and high power lasers as well as to form non-absorbing mirrors for high power lasers.

The known quantum well intermixing methods have some drawbacks. For example, one method (Impurity Induced Disordering) requires the introduction of impurities, another (Impurity-free Vacancy Disordering) is not capable of high spatial resolution and yet another laser irradiation induced disordering is only applicable to certain specific semiconductors. The known methods also

require complicated preparation of samples which in turn reduces throughput and increases costs.

Object of the Invention

It is therefore an object of the present invention to at least partially mitigate the difficulties experienced with prior art quantum well intermixing methods.

It is a further object of the present invention to provide a method of integrating optoelectronic or photonic circuit using a novel quantum well intermixing technique.

Summary of the Invention

According to a first aspect of the present invention there is provided a method of manufacturing a photonic integrated circuit comprising a structure having a quantum well region, and performing quantum well intermixing on said structure, characterised in that said step of performing quantum well intermixing comprises exposing at least a first portion of said structure to a plasma, and annealing said structure.

According to a second aspect of the present invention there is provided a method of controlling the bandgap energy of a photonic

interpolated circuit by plasma-induced layer intermixing of a first portion of said circuit whereby an absorption or lasing wavelength of said circuit is modified.

Preferably, the method further comprises forming an annealing cap on said portion of said structure.

Advantageously said annealing step comprises sandwiching said structure between two pieces of substrate.

Conveniently, the exposing step comprises exposing said portion of said structure at a process pressure at which said quantum well intermixing is optimal.

In a preferred embodiment the structure is a compound semiconductor quantum well structure.

One example is a $In_xGa_{1-x}As/In_xGa_{1-x}As_yP_{1-y}$ structure.

According to a second aspect of the invention, there is provided a quantum well intermixing process comprising exposing a quantum well structure to a plasma, and thereafter annealing said structure.

Conveniently the process further comprises forming an annealing cap on said structure.

Advantageously said annealing step comprises sandwiching said structure between two pieces of substrate.

Preferably said exposing step comprises exposing said structure at a process pressure at which said quantum well intermixing is optimal.

Preferably said structure is an $In_xGa_{1-x}As/In_xGa_{1-x}As_yP_{1-y}$ structure.

Brief Description of the Drawings

An exemplary embodiment of the invention will now be described with reference to the accompanying drawings in which:-

Figure 1 shows a schematic diagram of a quantum well structure with a graphical representation of the bandgap energy;

Figure 2 shows the bandgap shift plotted against exposure time for different microwave powers;

Figure 3 shows the full wave at half maximum of photoluminescence for different microwave powers;

Figure 4 shows the variation of bandgap energy shift with process temperature;

Figure 5 shows the bandgap energy shift as a function of process pressure;

Figure 6 shows the shift of photoluminescence from samples exposed to plasma sustained by radio frequency only;

Figure 7 shows the variation in photoluminescence from samples exposed to plasma sustained by microwave only;

Figure 8 shows a schematic cross-sectional view through a sample half masked with photoresist;

Figure 9 shows the photoluminescence signal obtained from the sample of Figure 8 after exposure and annealing;

Figure 10 shows the relative bandgap energy shift for samples exposed to plasma with different oxide cap thickness;

Figure 11 illustrates the epitaxial growth and regrowth technique;

Figure 12 shows the selective area epitaxy technique;

Figure 13 shows the effect of quantum well intermixing.

Description of the Preferred Embodiments

Referring first to Figure 1, an In_xGa_{1-x} As/$In_xGa_{1-x}As_yP_{1-y}$ structure (10) was grown using metal organic chemical vapour deposition (MOCVD) on a lower InP cladding layer (12) on an InP substrate. A single undoped quantum well region (14) was formed, consisting of a 5.5 nm wide $GaIn_xAs$ quantum well, with 12 nm $GaIn_xAs_yP$ (λ_g=1.26μm) barriers (16,18). The active region was bounded by step graded index (GRIN) $GaIn_xAs_yP$ confining layers (20-2, 24-6). The thickness and composition of these layers were 50nm of λ_g=1.18 μm and 80nm of λ_g=1.05 μm, respectively. The structure, which was lattice matched to InP throughout, was completed with a 1.4 μm InP upper cladding layer (28) and a layer (30) of 0.65 μm $GaIn_xAs_yP$ followed by a 0.1μm $GaIn_xAs$ layer (32) forming a contact layer. The lower cladding layer (12) was Sulfer-doped to a

concentration of $2.5x10^{18}$ cm^{-3}. The upper cladding layer (28) was doped with Zn to a concentration of $7.4x10^{17}$ cm^{-3} and the subsequent layers (30,32) were doped with $2x10^{18}$ cm^{-3} and $1.3x10^{19}$ cm^{-3} concentration of Zn respectively. The core of the waveguide was undoped, thus forming a P-I-N structure with its intrinsic region restricted to the quantum well and GRIN layers.1

The GRIN structure is used to produce better electron confinements and thus improving the optical confinement factor. The lower GRIN region (18, 24, 26) is doped with n-type sulfer to provide good current conduction. However, the upper GRIN region (16,20,22) is not doped with p-type Zn, as to do so would potentially allow Zn to diffuse into the quantum well region during rapid thermal processing (RTP).

The GaInAsP layer (30) is sandwiched between the upper cladding layer (28) and the contact layer (32) so as not to cause an abrupt change from InP structure to GaInAs structure, which is not lattice matched.

The variations in bandgap energy is diagrammatically shown in Figure 1b.

The samples were exposed to Ar-plasma, generated using an Electron Cyclotron resonance (ECR) system, at various process conditions. For a first sample set, during the plasma treatment, the microwave power was 1400 W and the RF power was 450W (self DC bias between -12 and -38V) with Ar flow rate of 50sccm and process pressure of 30mTorr. The exposure time was varied from 1 to 15 min. A second set of samples were exposed to the Ar plasma with the similar process conditions except that the microwave power was reduced to 800W (self DC bias between -57 and -63V). The exposure time was varied from 1 to 9 min.

After exposure, a 200 nm thick SiO_2 layer was deposited on the sample using plasma enhanced chemical vapor deposition (PECVD). This dielectric layer acts as an annealing cap preventing the outdiffusion of group V elements during annealing. The annealing was carried out using a rapid thermal processor at 600°C for 120s. During annealing, the sample was sandwiched between two pieces of fresh GaAs substrate to provide an As overpressure. Photo-luminescence measurements were performed at 77 K on samples both before and after annealing to assess the degree of bandgap energy shift, as a measure of quantum well intermixing.

Figure 2 shows the bandgap energy shift as a function of exposure time for samples exposed to process with microwave powers of 1400W and 800W respectively. As can be seen, the degree of intermixing increases gradually with increasing exposure time for samples exposed to 1400W. The bandgap shift saturates at about 72meV after 10min of Ar-plasma treatment. This implies that the maximum density of point defects generated by both ion bombardment and radiation damages saturate after an exposure time of about 10min. The samples exposed to 800W produced results with similar trend to that of 1400W, but with lower degrees of bandgap shift. This might be due to the fact that at lower microwave power, and hence lower Ar plasma density, the defect density generated by both physical and radiation damage will be lower. The highest attainable bandgap shift under these exposure conditions was found to be around 42meV for samples treated for 9 minutes.

The full wave at half maximum (FWHM) of the photoluminescence curves were also measured and broadening relative to the as grown samples was plotted in Figure 3. From the graph, the maximum broadening of the photoluminescence curve was about 17nm for samples exposed to the plasma at microwave power of 1400W for 10 minutes. The broadening can be regarded as relatively small. It

can therefore be concluded that the quality of the quantum structures remain relatively high after being intermixed using this technique.

Experiments were carried out to study the effect of process pressure and the cathode temperature on quantum well intermixing of the InGaAs/InGaAsP laser structure. The samples were exposed for 1 minute, at temperature range between 30°C and 300°C and pressure range between 10 and 70 mTorr, with microwave and RF powers set to 1400W and 450W.

Figure 4 shows the bandgap energy shift with respect to different exposure temperatures. Samples treated at higher temperatures show differential bandgap shifts of about ~10meV, whilst samples exposed to the plasma with cathode temperature of 100°C give a maximum bandgap shift of ~20meV. It is normally expected that samples implanted at high temperature result in larger degrees of intermixing. The present observations indicate therefore that ion-bombardment-induced quantum well intermixing is not a prominent mechanism to the intermixing process of the invention.

Figure 5 shows the differential bandgap energy shift as a function of process pressures. A maximum bandgap shift of ~30meV

was observed from sample processed at a chamber pressure of 30mTorr, reducing at pressures lower or greater than 30mTorr. At low pressure, the plasma density is low, hence creating a lower degree of point defects density due to both ion-bombardment and plasma radiation. However as pressure increases, the mean free path of the ion decreases, thus ions become less energetic and produce lower degree of bombardment damage and hence lower degrees of quantum well intermixing. From Fig 5, the optimum process pressure for this quantum well intermixing technique is therefore found to be 30mTorr.

In order to study the effects of ion bombardment and plasma radiation damage on quantum well intermixing in this material system, the samples were exposed to plasma sustained by only RF power and only microwave oscillation. The plasma generated using RF power only is expected to dominantly create ion bombardment damage. This is mainly due to the high potential difference (i.e. ~ 130eV) between the plasma and the semiconductor. On the other hand, plasma radiation induced damage is expected to dominate in the microwave-only processes as the plasma glow under these conditions is subjected to no acceleration field.

Figure 6 shows the results from samples exposed to plasma sustained by RF-only, and Fig 7 the microwave-only conditions. As can be seen from Figure 6, samples treated under RF-only conditions exhibit insignificant bandgap shift, i.e. a maximum of 19 meV. On the other hand, in Figure 7, differential bandgap shift as large as 42meV was observed from samples exposed to microwave-only conditions. These results imply that high-energy radiation generated by high density electron cyclotron resonance plasma plays an important role in quantum well intermixing in the InGaAs-InGaAsP structures using the present quantum well intermixing process.

To further verify the above observations, InGaAs/InGaAsP samples were exposed to UV light of $15W/m^2$ generated using a mask aligner with a mercury lamp for up to 10 minutes followed by annealing. No significant bandgap shift was, however, observed in these samples. This might be because the i-line from the mask aligner is not of high enough energy to generate a significant level of bond disruption to the lattice.

In order to study the selectivity of the process, samples of 2 x $4mm^2$, with half of the area masked with photoresist, were prepared (Figure 8). These samples were exposed to Ar plasma

with RF 450W and microwave of 1400W for 5 minutes. The region protected with photoresist acted as the quantum well intermixing mask, whereas the area exposed to Ar-plasma was intermixed after annealing.

Figure 9 shows the photoluminescence signal obtained from the sample after Ar exposure and subsequent thermal annealing.
To subsequently verify the quantum well intermixing mechanisms of this process, InGaAs/InGaAsP samples deposited with thickness of SiO_2 between 100nm and 1200nm were exposed to Ar-plasma generated using RF 450 (dc bias of around 100V) and microwave 1400W for 10 minutes. The SiO_2 cap was removed using HF solution prior to quantum well intermixing.

Figure 10 shows the relative bandgap energy shift for samples exposed to Ar plasma with different SiO_2 cap thickness. It was found that the differential shift of the intermixed samples stays constantly at a maximum of around 50meV for samples deposited with SiO_2 thickness of thinner than 500nm. From calculation, the penetration range of Ar ions, with energy of ~100eV, in SiO_2 film is not expected to be greater than 10nm. This implies that the quantum well intermixing effect observed from samples capped with <500nm of SiO_2 is therefore mainly resulted from the plasma

irradiation. A gradual decrease in bandgap shift was however observed from samples capped with SiO_2 greater than 500nm. Quantum well intermixing was inhibited from samples capped with SiO_2 thickness of greater than 800nm. This is expected as the radiation will be severely scattered and absorbed when passing through a thick medium hence resulting in lower degree of quantum well intermixing.

The ability to control the degree of intermixing across a wafer, i.e. selected intermixing at selected area (SISA) effect of the process was also investigated. This effect was achieved by controlling the regions of exposure, and hence concentration of point defects and degree of quantum well intermixing, by varying the exposure windows using photoresist. This technique allows the fabrication of multiple section devices such as superluminescent diodes using a one-step processing technique.

Although the embodiment has been described in the context of an Ar plasma, and a particular compound semiconductor, it will be understood by those skilled in the art that other plasma gases may be used, and that the technique is applicable to other semiconductors. The use of ECR to provide the plasma is one advantageous possibility, but other systems such as RF, DC or ICP

systems could be used. For annealing, a furnace can be used instead of RTP.

Claims:

1. A method of manufacturing a photonic integrated circuit comprising a structure having a quantum well region, and performing quantum well intermixing on said structure, characterised in that said step of performing quantum well intermixing comprises exposing at least a first portion of said structure to a plasma, and annealing said structure.

2. The method of claim 1 wherein said exposing step comprises exposing said portion of said structure using process conditions at which said quantum well intermixing is optimal.

3. A method of controlling the bandgap energy of a photonic interpolated circuit by plasma-induced layer intermixing of a first portion of said circuit whereby an absorption or lasing wavelength of said circuit is modified.

4. A method as in any preceding claim, comprising generating said plasma by electron cyclotron resonance.

5. A method as in any of claims 1-3, comprising generating said plasma by a radio-frequency plasma system.

6. A method as in any of claims 1-3, comprising generating said plasma by a direct current plasma system.

7. A method as in any of claims 1-3, comprising generating said plasma by an inductively coupled plasma system.

8. A method as in any preceding claim, wherein said plasma comprises an Ar plasma.

9. A method as in any preceding claim, further comprising providing a mask to prevent intermixing of a second portion of said structure.

10. The method of claim 9, wherein said mask comprises a photoresist.

11. The method of claim 9, wherein said mask comprises a dielectric layer.

12. The method of claim 9, wherein said mask comprises a metal layer.

13. The method of any of claims 1-8, further comprising providing a mask over at least a part of said first portion to control the amount of quantum well intermixing.

14. The method of claim 13, wherein different mask densities are used to provide differential quantum well intermixing.

15. The method of any preceding claim, wherein said annealing step comprises annealing said structure at optimum annealing conditions for quantum well intermixing.

16. The method of claim 15, further comprising forming an annealing cap on said portion of said structure.

17. The method of claim 14, wherein said portion of said structure remains bare during annealing.

17. The method of any preceding claim, wherein said annealing process is carried out with an overpressure of impurities.

18. The method of any preceding claim, wherein said structure is a compound semiconductor quantum well structure.

19. The method of any preceding claim wherein said structure is an In_xGa_{1-x} As/$In_xGa_{1-x}As_yP_{1-y}$ structure.

PLASMA PROCESS FOR PHOTONIC INTEGRATED CIRCUIT

ABSTRACT OF THE DISCLOSURE

A method of manufacturing a photonic integrated circuit including quantum wells, comprises the step of quantum well intermixing by subjecting the quantum well region to a plasma, eg. an Argon plasma, followed by annealing the structure, to achieve a desired bandgap.

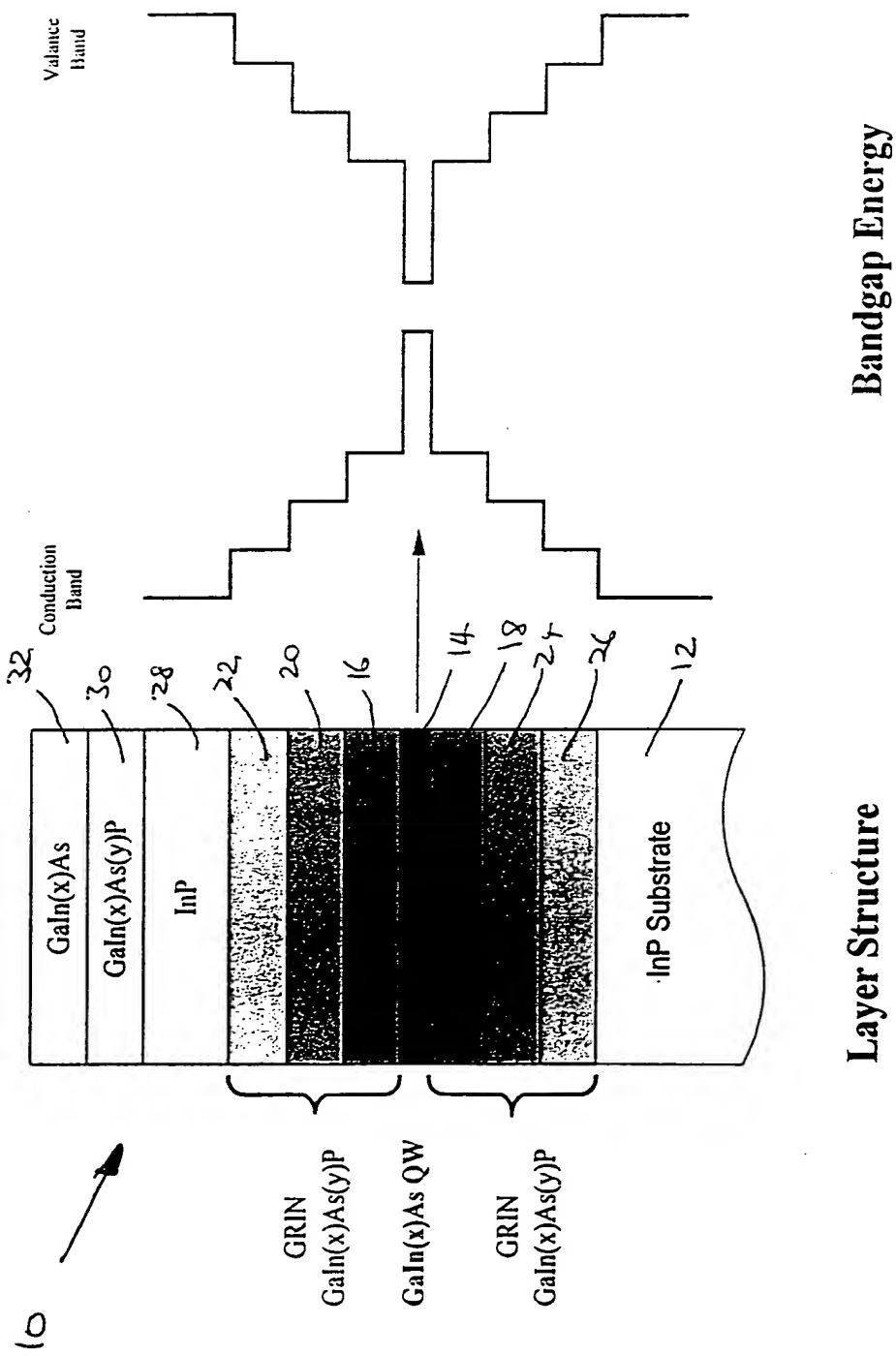
Valance Band
Conduction Band
32
30
28
22
20
16
14
18
24
26
12
GaIn(x)As
GaIn(x)As(y)P
InP
InP Substrate
GRIN GaIn(x)As(y)P
GaIn(x)As QW
GRIN GaIn(x)As(y)P
10
Bandgap Energy
Layer Structure

Figure 1

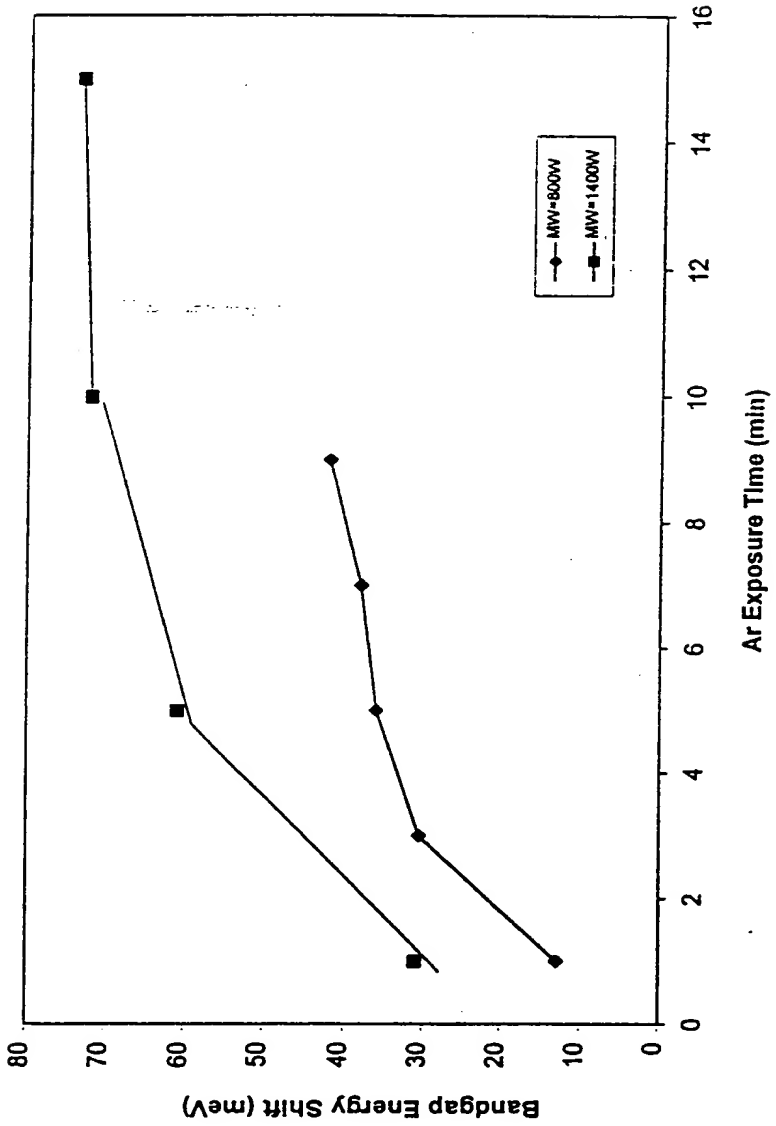
Bandgap Energy Shift (meV)
0
10
20
30
40
50
60
70
80
0
2
4
6
8
10
12
14
16
Ar Exposure Time (min)
MW=800W
MW=1400W

Figure 2

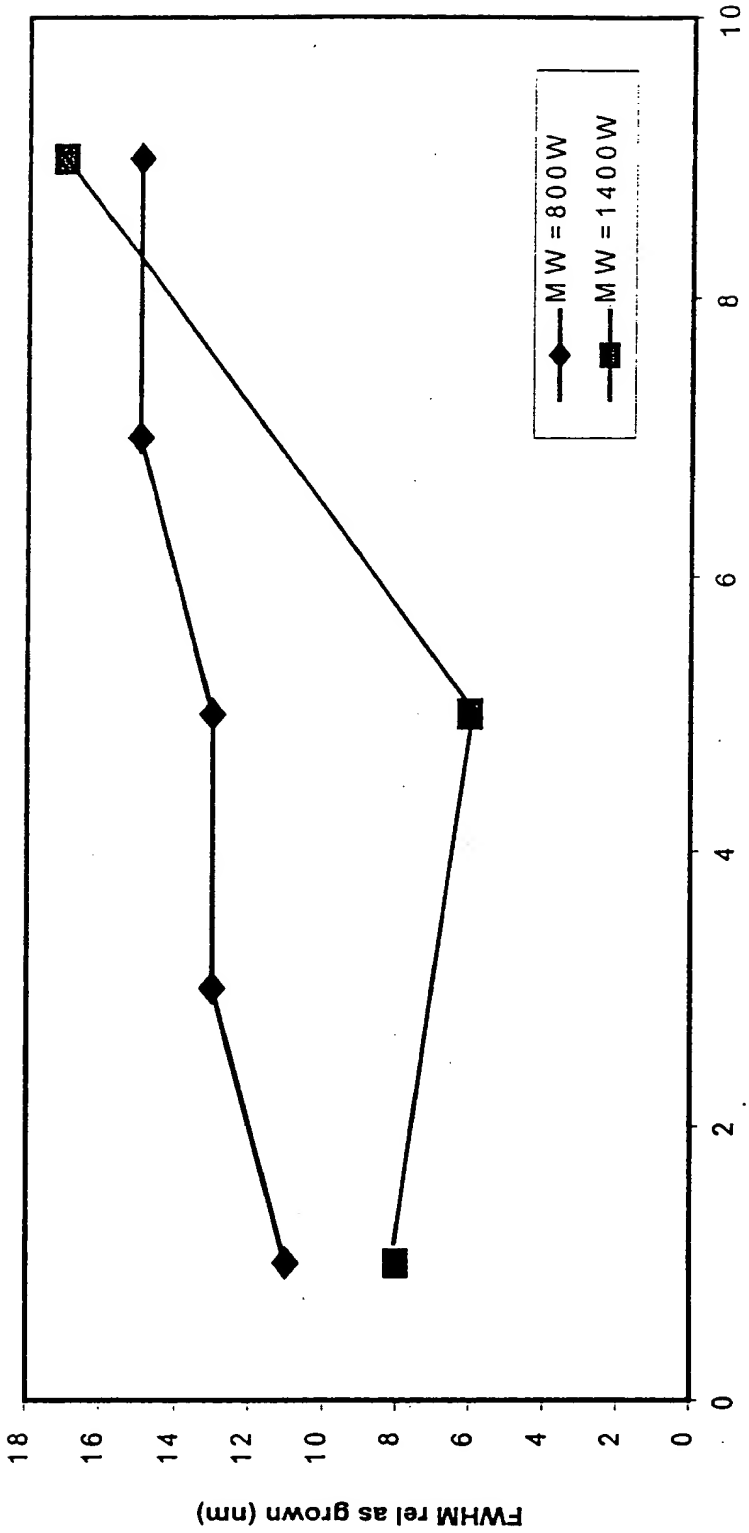
FWHM rel as grown (nm)
0
2
4
6
8
10
12
14
16
18
0
2
4
6
8
10
Ar Exposure Time (mIn)
MW=800W
MW=1400W

Figure 3

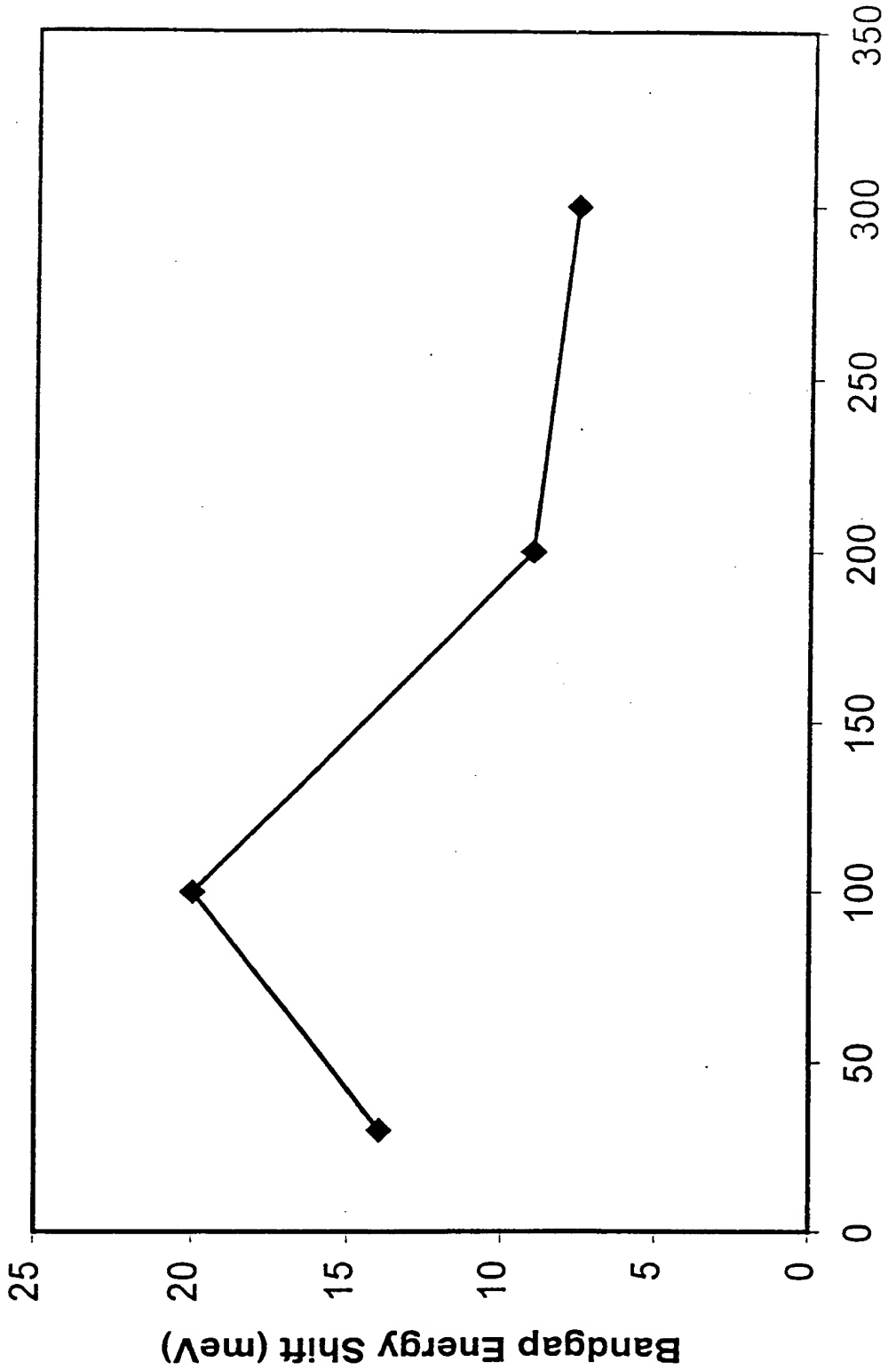
Bandgap Energy Shift (meV)
25
20
15
10
5
0
0
50
100
150
200
250
300
350
Temperature (degree)

Figure 4

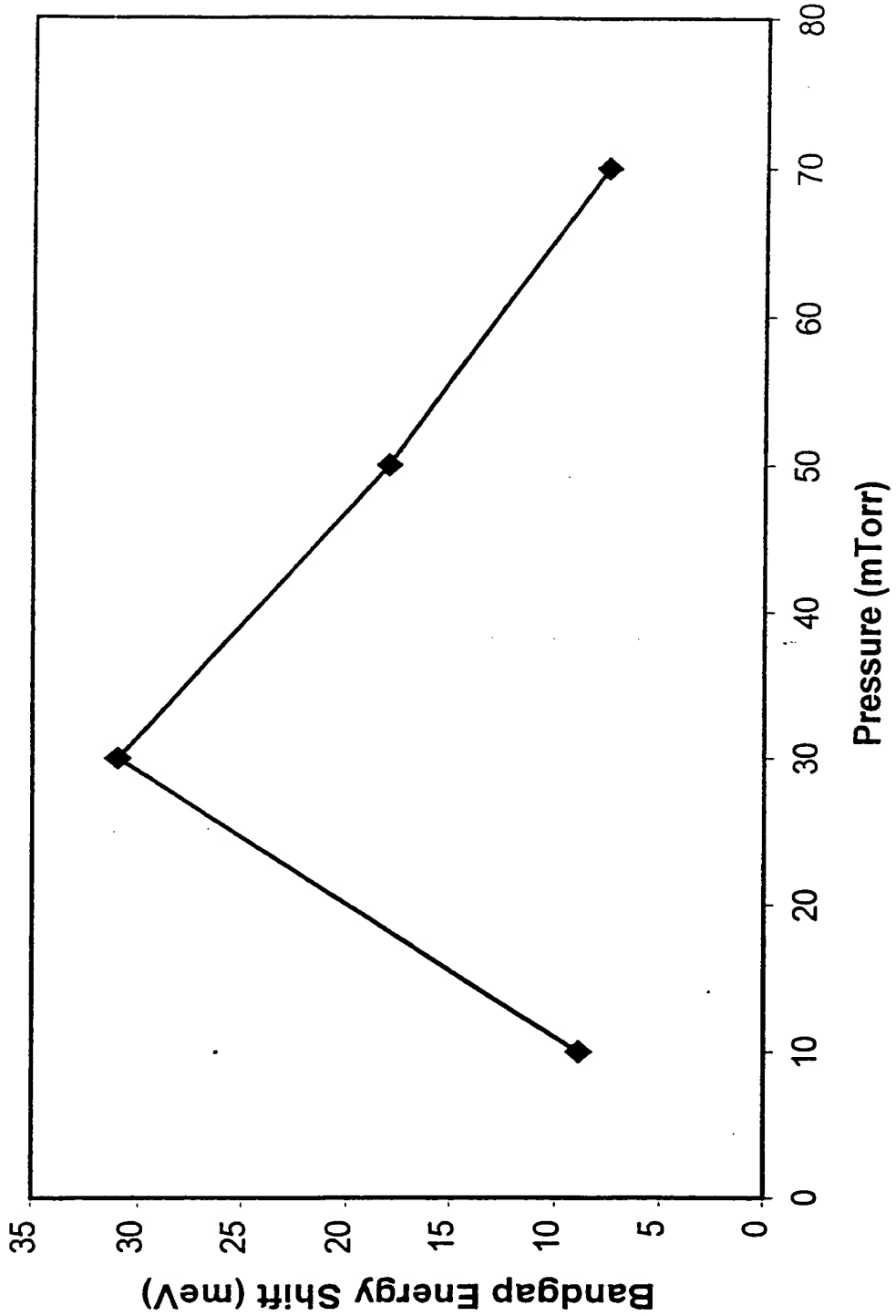
Bandgap Energy Shift (meV)
0
5
10
15
20
25
30
35
Pressure (mTorr)
0
10
20
30
40
50
60
70
80

Figure 5

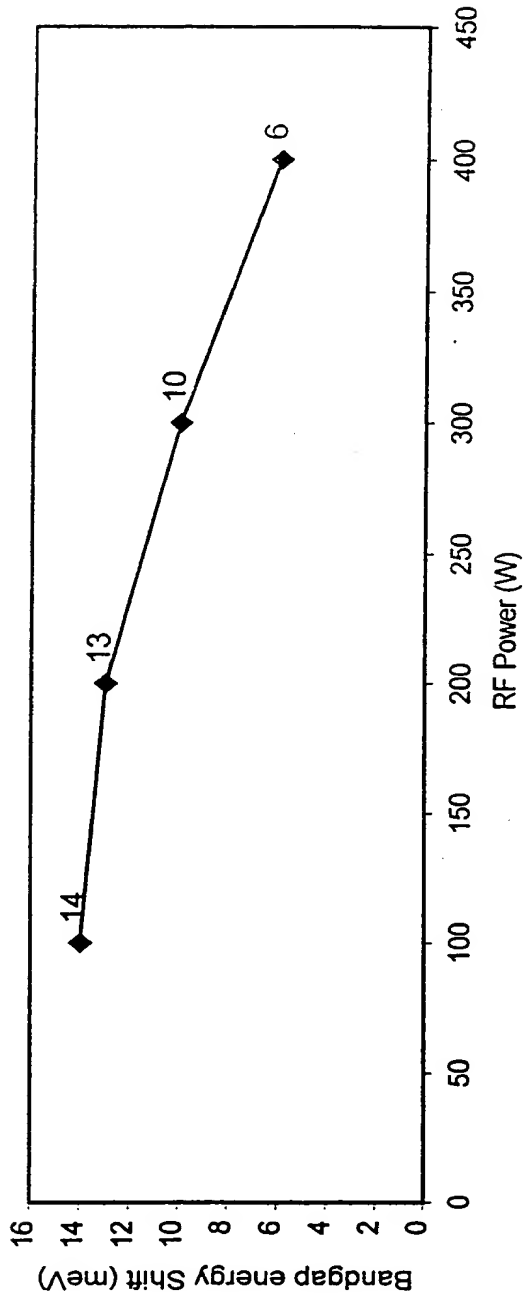

Figure 6

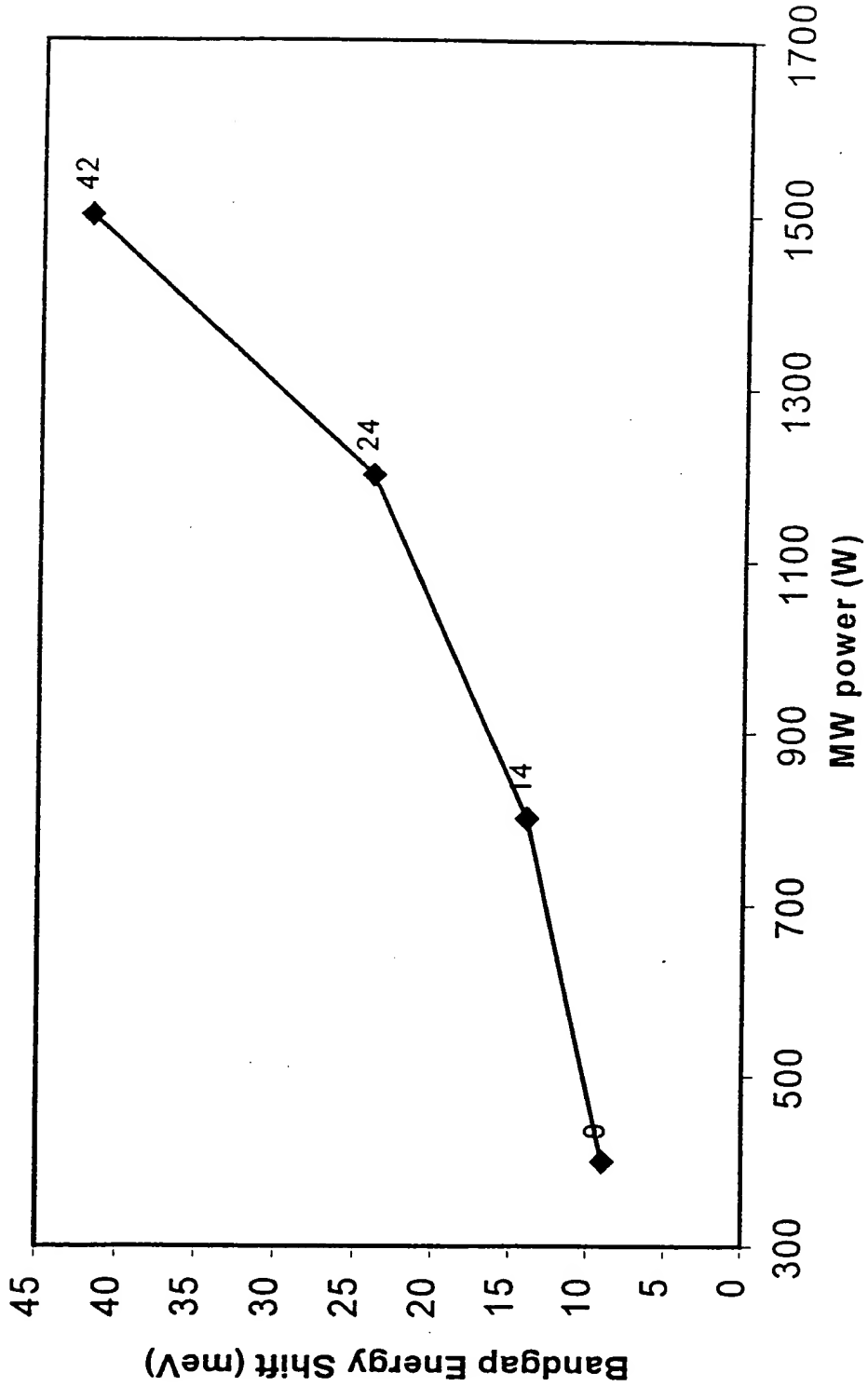
Bandgap Energy Shift (meV)
0
5
10
15
20
25
30
35
40
45
MW power (W)
300
500
700
900
1100
1300
1500
1700
42
24
14
9

Figure 7

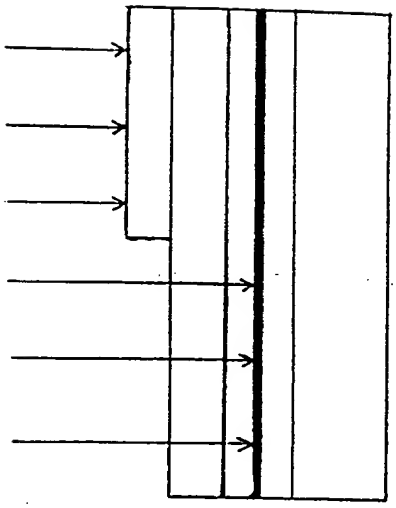

Figure 8

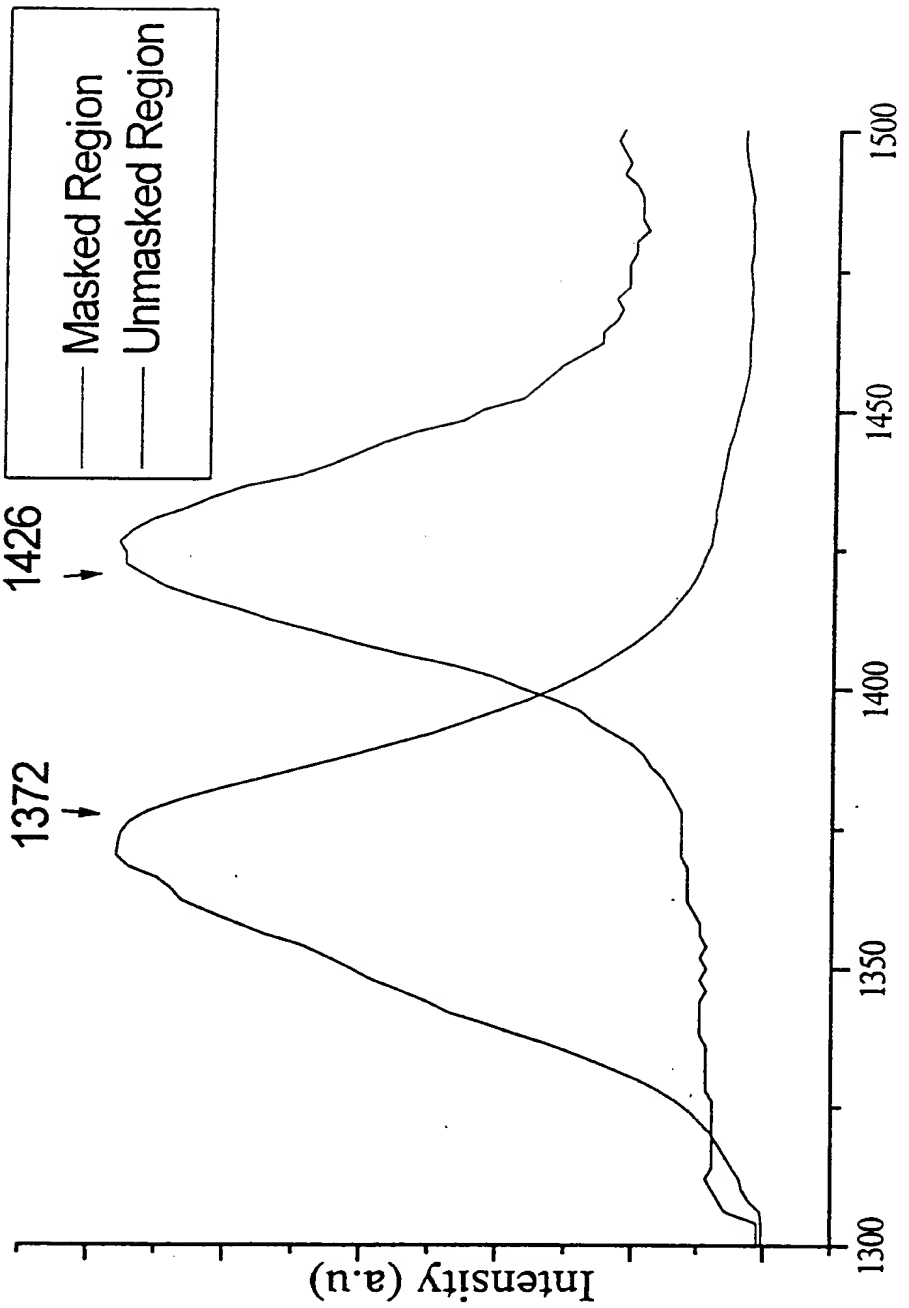
Masked Region
Unmasked Region
1426
1372
Intensity (a.u)
1300
1350
1400
1450
1500
Wavelength (nm)

Figure 9

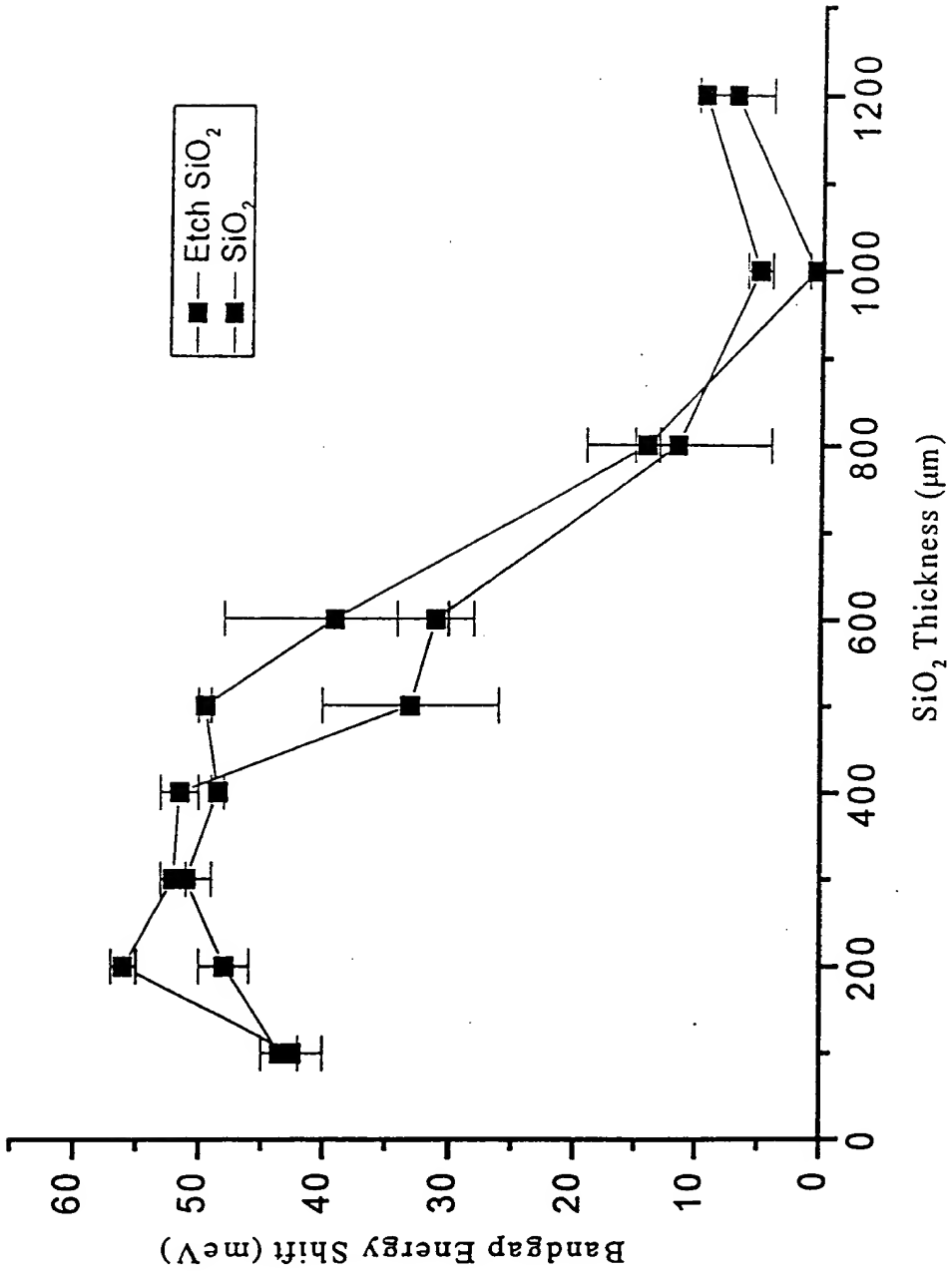
Etch SiO_2
SiO_2
Bandgap Energy Shift (meV)
0
10
20
30
40
50
60
0
200
400
600
800
1000
1200
SiO_2 Thickness (μm)

Figure 10

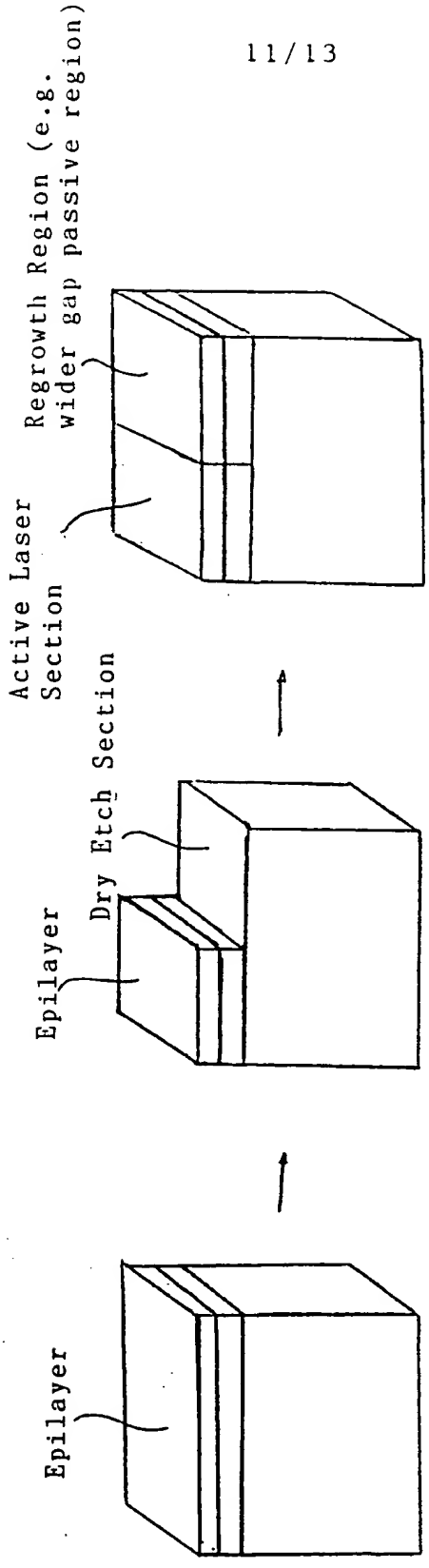
Epilayer
(a)
Epilayer
Dry Etch Section
(b)
Active Laser Section
Regrowth Region (e.g. wider gap passive region)
(c)

FIGURE 11

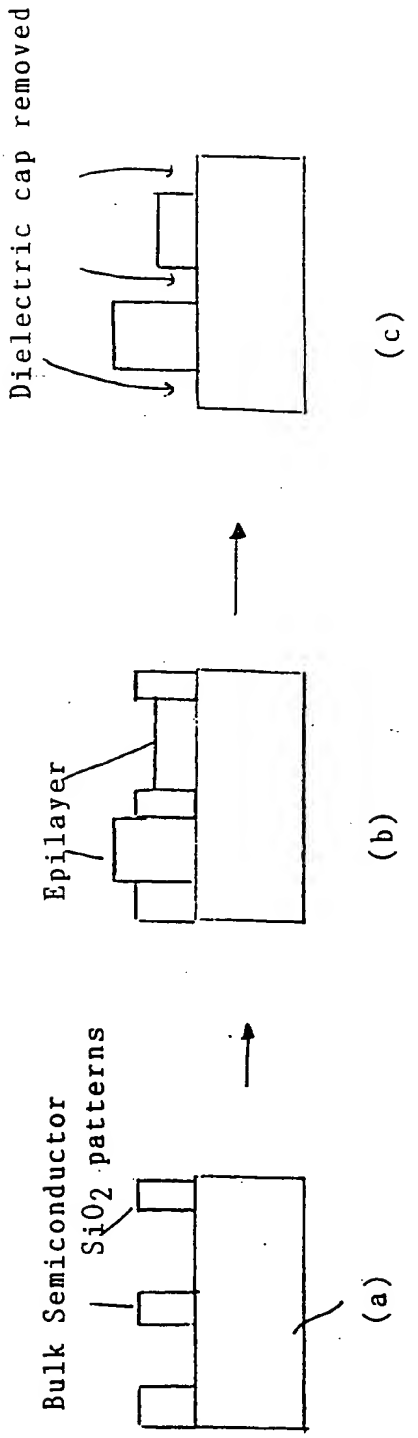
Bulk Semiconductor
SiO_2 patterns
(a)
Epilayer
(b)
Dielectric cap removed
(c)

FIGURE 12

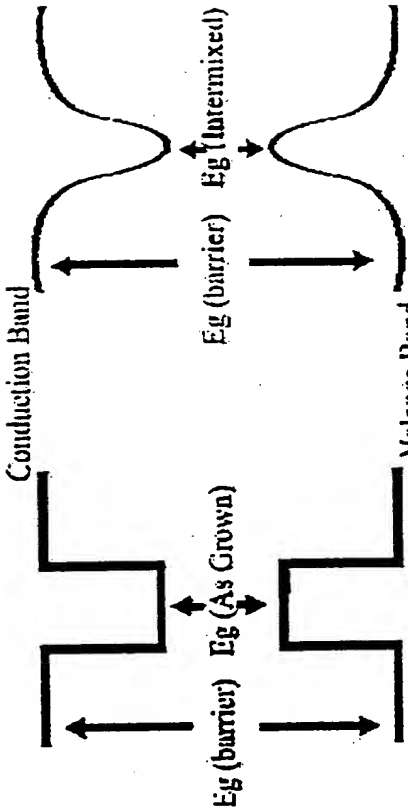
Conduction Band
Eg (barrier)
Eg (Intermixed)
Eg (As Grown)
Eg (barrier)
Valance Band

Figure 13